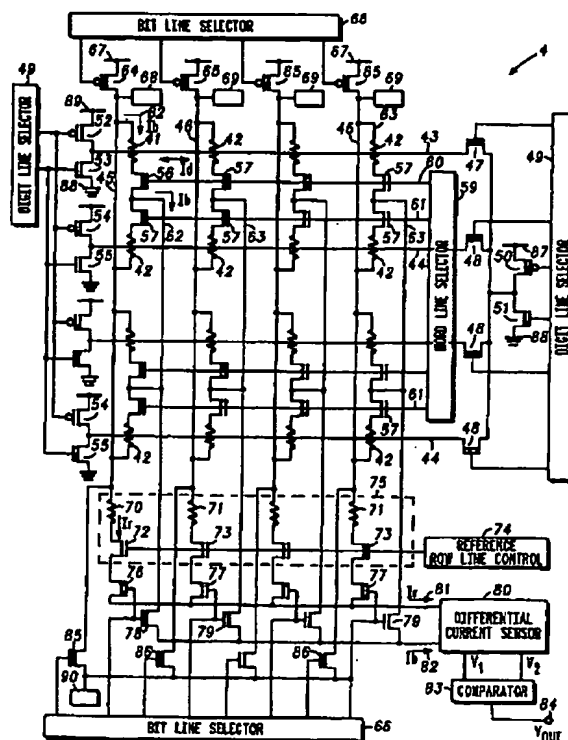# PCT

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(54) Title: MAGNETIC RANDOM ACCESS MEMORY WITH A REFERENCE MEMORY ARRAY

(57) Abstract

An MRAM device (4) includes a memory array and a reference memory array (75). The memory array arranges magnetic memory cells (41, 42) in rows and columns for storing information, and the reference memory array forms reference memory cells (70, 71) for holding a reference information in a row line. The magnetic memory cell has a maximum resistance $(R+\Delta R)$ and a minimum resistance (R) according to magnetic states in the cell. Each reference memory cell has a magnetic memory cell (70, 71) and a transistor (72, 73), which are coupled in series and have a reference resistance across the reference memory cell and the transistor. The transistor is controlled by a reference row line control (74), so as for the reference resistance to show a mid-value between the maximum resistance and the minimum resistance of the magnetic memory cell. A bit line current (Ib) and a reference bit current (Ir) are provided to the magnetic memory cell and the reference memory cell, respectively. Magnetic states alternates the bit line current, which is compared to the reference bit current to provide an output.

MAGNETIC RANDOM ACCESS MEMORY WITH A REFERENCE MEMORY ARRAY

Field of the Invention

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The present invention relates to a magnetic random access memory, and more particularly, to a magnetic random access memory with a reference memory array.

Background of the Invention

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A magnetoresistive random access memory (MRAM), which is one of non-volatile memory devices, includes a plurality of magnetic memory cells. It is known that the magnetoresistive effect appears in multi-layer films that are alternately stacked by magnetic layers and non-magnetic layers. Magnetic resistance over a

15 magnetic memory cell indicates minimum and maximum values when magnetization vectors in magnetic layers point in the same or opposite directions, respectively. The same and opposite directions of magnetization vectors in two magnetic layers are called "Parallel" and "Anti-parallel" states, respectively. When magnetic material is employed for a memory device, Parallel and Anti-parallel directions, for example, are

20 logically defined as "0" and "1" states, respectively. The magnetization vectors in magnetic layers are very quickly switched to another direction by an application of a magnetic field over a switching point, and maintain the magnetization direction even without a magnetic field.

The MRAM device normally has magnetic memory cells arranged on

25 intersections of metal lines, which are placed in rows and columns. The MRAM circuit shows an MRAM bank that has bit lines, a reference line, and digit lines. The reference line is placed parallel with bit lines and perpendicular to digit lines. On each intersection of these lines, memory cells and reference cells are arranged in rows and columns. The reference cell is employed to sense states stored in the memory cell.

30 The MRAM device generally is formed on a substrate such as a semiconductor or glass. Magnetic and non-magnetic layers are sequentially deposited on the substrate and etched to form magnetic memory cells, which are 0.2 μm by 0.3 μm in size, for instance. The magnetic layer usually has a 10-100Å thickness while the non-magnetic layer is 10-30Å thick. The MRAM device includes magnetic memory cells for

35 storing specific information, and reference magnetic memory cells where a reference state is maintained. In order to read states stored in a magnetic memory cell (active or target cell), a sense current and a reference current are applied to the target cell and a reference magnetic memory cell (reference cell), respectively. The target and reference cells generate voltage drops across the cells that correspond to magnetic

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resistance values of the target and reference cells, respectively. These voltages are compared to each other to determine states in the target cell. Therefore, it is desirable to provide an MRAM device that has magnetic memory cells without relative variations of the magnetic resistance to correctly compare a target cell to a reference

5   cell.

        Accordingly, it is a purpose of the present invention to provide an improved MRAM device that has a high-speed, high-density, and low power memory.

        It is another purpose of the present invention to provide an improved MRAM device that has a high reliability reading process.

10   It is still another purpose of the present invention to provide an improved MRAM device that reduces variations of the magnetic resistance in magnetic memory cells.

Summary of the Invention

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        These needs and others are substantially met through provision of a magnetoresistive random access memory (MRAM) device that includes a reference memory array. The MRAM device has a plurality of magnetic memory cells placed on intersections of bit lines and digit lines. The reference memory array has a plurality of

20   reference cells and resistive elements. Each reference cell is coupled in series to a resistive element. A total resistance across the reference cell and the resistive element is set to a resistance between a maximum resistance and a minimum resistance of the target cell, thereby it is possible to compare the magnetic resistance of the target cell to one of the reference cell to provide an output. The total resistance

25   is typically a mid-point between maximum and minimum resistance values.

Brief Description of the Drawings

        FIG. 1 shows a basic circuit formed in an MRAM device on a reading mode;

30   FIG. 2 shows a simplified and enlarged magnetic memory cell with magnetic layers separated by a non-magnetic layer;

        FIG. 3 shows a graph illustrating hysteresis characteristics of the magnetic memory cell described in FIG. 2;

        FIG. 4 shows an MRAM device circuit; and

35   FIG. 5 shows an another MRAM device circuit.

Detailed Description of the Preferred Embodiments

        FIG. 1 shows a basic circuit 1 illustrating a reading operation in an MRAM

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resistance of the cell 2. Assuming cell 2 is in the state that magnetization vectors in layers 31 and 32 point in the Parallel state (same direction) under no external magnetic field, the external magnetic field changes to a value H1 moving to the right along the abscissa. As shown by curve 36, magnetization vectors in second magnetic

5   (free) layer 32 are switched to the left at a magnetic field H1 and magnetization vectors in layers 31 and 32 are oriented in the Anti-parallel state (opposite direction) as indicated by arrows 37. Consequently, a magnetic resistance of cell 2 increases from R by ΔR. Next changing the magnetic field from H1 as shown by curve 38, magnetization vectors in second magnetic layer 32 are switched at a magnetic field

10   H2 to the right. Consequently the magnetic resistance is lowered to R by ΔR and magnetization vectors in layers 31 and 32 point in the Parallel direction as indicated by arrows 39. An example of the memory cell structure is shown in U.S. Patent No. 5,768,181.

Referring to FIG. 1 again, selector 10 provides a word signal on word line 13

15   and a bit signal on bit line 14, which allow switching transistors 16, 17, and 19 to turn on and bit current Ib to flow in target cell 11. Target cell 11 determines a magnitude of current Ib, which depends on magnetic states stored in target cell 11. Reference element controller 21 provides a resistance control signal on reference row line 22 to control a drain-source resistance of transistor 18. In order for comparator 25 to

20   compare states in target cell 11 to states in reference cell 12, transistor 18 establishes a total resistance across reference element 20 between a maximum resistance (R+ΔR) and a minimum resistance (R) of target cell 11, which typically is a mid-point resistance value that is equal to R+ΔR/2. Current Ib and current Ir are converted to voltages V1 and V2, respectively, which are compared at comparator 25 to provide

25   output voltage Vout at output terminal 30. When current Ib is smaller than current Ir, that is, voltage V1 is lower than voltage V2, comparator 25 gives a low voltage at terminal 30, which means target cell 11 has a maximum resistance (R+ΔR) and is in the "Antiparallel" state. On the contrary, when voltage V1 is higher than voltage V2, comparator 22 provides a high voltage at terminal 30, which means target cell 11 has

30   a minimum resistance (R) and is in the "Parallel" state.

As mentioned earlier, transistor 18 is controlled for the total resistance of reference cell 12 and transistor 18 to create a resistance between the maximum and the minimum resistances of the magnetic memory cell. That enables comparator 25 to determine magnetic states stored in target cell 11.

35   Referring to FIG. 4, a circuit 4 for an MRAM device is described. A plurality of magnetic memory cells 41 and 42 are placed in rows and columns on intersections of digit lines 43 and 44 and reference bit lines 45 and 46. Digit lines 43 and 44 are coupled to transistors 47 and 48 and transistors 50-55, respectively. A digit line

device. A selector 10 selects a target magnetic memory cell (target cell) 11 and a reference magnetic memory cell (reference cell) 12, which are asserted by a word line 13 and a bit line 14. These cells are the same structure, each having magnetic layers separated by a non-magnetic layer. The structure and its characteristics are

5   described in FIGS. 2 and 3, and the detail will be explained hereinafter. Target cell 11 is coupled in series to a current sensor 15 through switching transistors 16 and 17 while reference cell 12 is coupled in series to current sensor 15 through a transistor 18 and a switching transistor 19. Reference cell 12 and transistor 18 form a reference element 20. A reference element controller 21 is connected to transistor 18 through

10   reference row line 22, on which a resistance control signal is provided to determine a drain-source resistance of transistor 18. Current sensor 15 detects a bit current Ib on a bit line 23 and a reference current Ir on a reference bit line 24 and converts to voltages V1 and V2, respectively. Voltages V1 and V2 are applied to positive and negative inputs of a comparator 25, respectively. As shown in FIG. 1, current sensor

15   15, for example, is formed by resistors 26 and 27 and amplifiers 28 and 29. Bit current Ib flowing in resistor 26 generates a voltage drop across resistor 26, which is amplified by amplifier 28 to produce voltage V1. Current Ir is converted to V2 in the same way as current Ib. Outputs of current sensor 15 are coupled to comparator 25 where voltages V1 and V2 are compared to provide an output voltage Vout on an

20   output terminal 30.

FIGS. 2 and 3 show an isometric view of a simplified and enlarged magnetic memory cell 2, and hysteresis characteristics 35 of cell 2 in FIG. 2, respectively. It should be noted that other types of magnetic memory cells can be employed for the memory device. Cell 2 has three layers that include first and second magnetic layers

25   31 and 32 separated by a non-magnetic layer 33. First and second magnetic layers 31 and 32 use magnetic material such as CoFe and NiFeCo. Magnetization vectors in first magnetic layer 31, for example, are magnetically pinned by an antiferromagnetic layer (not shown) that is placed adjacent layer 31. Second magnetic layer 32, which is magnetically free, alternates magnetization vectors responding to an external

30   magnetic field. Non-magnetic layer 33, for example, is formed by an insulating material such as Al_2O_3 and has a thickness of around 20Å. The thin thickness allows non-magnetic layer 33 to form a tunneling junction between first and second magnetic layers 31 and 32, through which a tunneling current flows. As will be seen in FIG. 3, a magnetic resistance of the memory cell changes according to directions of

35   magnetization in second magnetic layer 32 that causes a tunneling current in non-magnetic layer 33 to vary. The magnetic layers would be patterned to substantially align the magnetization as shown in U.S. Patent No. 5,757,695.

Referring to FIG. 3 again, the abscissa of FIG. 3 indicates a direction and strength of a magnetic field applied to cell 2. The ordinate represents the magnetic

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selector activates one of digit lines 43 and 44, and determines directions of the digit
current. Pairs of transistors 50 and 51, 52 and 53, and 54 and 55 determine current
directions of the digit current. Cells 41 and 42 are coupled in series to switching
transistors 56 and 57, respectively. Gate electrodes of transistors 56 and 57 are
5   coupled to word line selector through word lines 60 and 61.

Reference bit lines 45 and 46 are placed perpendicularly to digit lines 43 and
44, which are coupled to transistors 64-65, respectively. Gate electrodes of
transistors 64 and 65 are coupled together to bit line selector 66, while drain
electrodes of transistors 64 and 65 are coupled to a power line 67. Programming
10   current sources 68 and 69, which supply a writing current to a magnetic memory cell,
are coupled to reference bit lines 45 and 46, respectively.

Reference bit lines 45 and 46 further are coupled to reference magnetic
memory cells (reference cells) 70 and 71, which have the same memory structure as
cells 41 and 42. Reference cells 70 and 71 are coupled in series to transistors 72 and
15   73, respectively. Gate electrodes of transistors 72 and 73 are linked together to a
reference row line control 74 that controls a drain-source resistive value of transistors
72 and 73. Reference cells 70 and 71 and transistors 72 and 73 form a row line
memory array 75 as shown by a dashed line. Reference cells 70 and 71 are
equivalent to reference cell 12 in FIG. 1 while transistors 72 and 73 are equivalent to
20   transistor 18. Transistors 72 and 73 are coupled to transistors 76 and 77,
respectively. Bit lines 62 and 63 are coupled in series to transistors 78 and 79,
respectively. Source electrodes of transistors 76 and 77 are connected together to
current sensor 80 to provided a reference current Ir indicated by an arrow 81 and also
source electrodes of transistors 78 and 79 are connected together to current sensor
25   80 to provide a bit current Ib expressed by an arrow 82. Outputs of sensor 80 are
coupled to comparator 83 to provide an output voltage Vout at an output terminal 84.
Current sensor 80 and comparator 83 are equivalent to sensor 15 and comparator 22
in FIG. 1. Transistors 85 and 86, which are controlled by bit line selector 66 on a
writing mode, are coupled to reference bit lines 45 and 46, respectively.
30   Next, a reading mode is carried out according to the following steps, which
sense target cell 41, for example. First, word line selector 59 provides a word signal
on word line 60 in order to turn transistor 56 on. Reference row line control 74 sends
a resistance control signal to transistor 72, which gives a mid-point resistance value
(that is equal to R+ΔR/2) across reference cell 70 and transistor 72. Finally bit line
35   selector 66 applies a signal to turn on transistor 76 and 78, and a signal for activating
reference bit line 45 to transistor 64, thereby transistors 64, 76, and 78 are all turned
on. Consequently, activation of transistors 56, 64, 72, 76, and 78 forms the same
circuit in MRAM device circuit 4 as the basic circuit of FIG. 1, and allows bit current Ib
and reference bit current Ir to flow in bit line 62 and reference bit line 45. That is, bit

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current Ib flows from power line 67 through transistor 64, target cell 41, transistors 56 and 78 to current sensor 80, and reference bit current Ir flows from power line 67 through transistor 64, cell 81, transistors 72 and 76 to current sensor 80.

As mentioned earlier in FIG. 1, bit current Ib and refernce bit current Ir change
5   based on states stored in cell 41. Current sensor 80 converts these currents Ib and Ir to voltages V1 and V2, respectively, which go to comparator 83. Comparator 83 compares voltage V1 to voltage V2 to give an output voltage Vout at output terminal 84. Generally, output terminal 84 is coupled to a data bus (not shown in FIG. 4) in a computer system.

10   In order to write states in a magnetic memory cell, a digit current and a bit current are applied to a digit line and a reference bit line. The digit current and the bit current generate magnetic fields, respectively, a combined magnetic field of which is sufficient enough to change states in the cell. Directions of the combined magnetic field determine states to be stored in the cell. When cell 41, for example, is accessed
15   to write states, digit line selector 49 turns transistor 47 on to activate digit line 43 and bit line selector 66 turns transistor 85 on to activate reference bit line 45. Transistors 56, 64, 76, and 78 are all turned off to prohibit from flowing a current into cell 41. Turning on transistor 85 allows the bit current to flow from current source 68 through reference bit line 45 and transistor 85 to a current sink 90. The bit current contributes
20   half of the combined magnetic field. Digit line selector 49 not only provides the digit current on digit line 43 but determines current directions according to states to be stored in cell 41. The digit current supports to produce another half of the combined magnetic field.

When a logic "0" is written in cell 41, digit line selector 49 turns transistors 50
25   and 53 on and transistors 51 and 52 off, thereby a digit current Id flows from a power line 87 through transistors 50 and 47, digit line 43 and transistor 53 to common line 88. Digit current Id allows the combined magnetic field to make the "Parallel" state in cell 41. Alternatively, when a logic "1" is stored in cell 41, transistors 51 and 52 are turned on and transistors 50 and 53 are turned off. Consequently, digit current Id is
30   provided on digit line 43 from a power line 89 through transistors 52, digit line 43 and transistors 47 and 51 to common line 87. This digit current supports the combined magnetic field to form the "Antiparallel" state in cell 41.

Referring to FIG. 5, another type of MRAM circuit 5 is illustrated. MRAM circuit 5 is the same as circuit 4 except shared bit lines 91 and 92, and a bit line selector 93.
35   Since MRAM circuit 5 includes shared bit lines, it attains MRAM device having less chip area and higher density. Portions of FIG. 5 that have the same reference numbers as FIG. 4 are the same as the corresponding elements in FIG. 4. Description for the same circuit configuration is omitted for simplicity.

Source electrodes of transistors 94 and 95, which correspond to transistor 75 in

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FIG. 4, are connected together to shared bit lines 91. Transistor 96 connects shared bit line 91 to differential current sensor 80 while shared bit line 92 coupled to differential current sensor 80 through transistor 97. Bit line selector 93 selects one of transistors 98-101 to provide a bit current and a reference bit current.

5   In an operation for reading memory cell 41, for instance, bit line selector 66 and 93 turn transistors 76, 96 and 98 on. At the same time word line selector 59 provides a word line signal to transistor 94, while reference row line control 74 sends a reference row line signal to transistor 72. Turning on transistors 98, 94, and 96 allows bit current Ib indicated by arrow 82 to flow from power line 67 through transistor 98,
10   cell 41, transistor 94, shared bit line 91 and transistor 96 to differential current sensor 80. And also reference bit current Ir expressed by arrow 81 is provided in reference cell 70, which flows through transistors 72 and 76 into current sensor 80.

          As mentioned earlier, differential current sensor 80 senses both currents Ib and Ir, and converts them to voltages V1 and V2, respectively. Comparator 83 compares
15   voltages V1 and V2 to provide output voltage Vout at output terminal 84 that corresponds to magnetic states stored in magnetic cell 41.

          Next, in order to read states in memory cell 42, transistors 99, 95, and 96 are turned on, thereby a bit current flows from power line 67 through transistor 99, cell 42, transistor 95, shared bit line 91, and transistor 96 to current sensor 80. That is,
20   shared bit line 91 is employed to sense not only cell 41 but cell 42. Further, magnetic memory cells 102 and 103 also use shared bit line 91 to provide a bit current from power line 67 to current sensor 80.

          In order to store states in memory cell 41, for example, bit line selector 66 turns on transistor 85 to access reference bit line 45, which allows current source 68 to
25   provide a bit current on reference bit line 45 to current sink 90. Further, digit line selector 49 controls transistors 47, 50-53 to give a digit current on digit line 43. These steps are the same process as described earlier for circuit 4 illustrated in FIG. 4.

          Thus, a new and improved MRAM device has been fully disclosed, which includes a reference memory array in a row line. The reference memory array
30   compensate and eliminate relative resistance variations of magnetic memory cells, which provides a steady reading function, high speed and high reliability.

What is claimed is:

1.   A magnetic random access memory comprising:
a first electrically conductive line;
a magnetic memory cell coupled in series to the first electrically conductive line, the magnetic memory cell having a magnetic resistance that is switched between a minimum magnetic resistance and a maximum magnetic resistance according to directions of magnetization vectors stored in the magnetic memory cell;
a second electrically conductive line;
a reference magnetic memory cell coupled in series to the second electrically conductive line, the reference magnetic memory cell having a predetermined magnetic resistance; and
a resistive element coupled in series to the reference magnetic memory cell, a total resistance across the reference magnetic memory cell and the resistive element being set between the minimum magnetic resistance and the maximum magnetic resistance.

2.   The magnetic random access memory as claimed in claim 1 further including a comparator having a first input and a second input, the first input being coupled to the first electrically conductive line and the second input being coupled to the second electrically conductive line, for comparing the magnetic resistance to the total resistance to provide an output.

3.   The magnetic random access memory as claimed in claim 2 wherein the comparator includes:
a converter for converting a first current on the first electrically conductive line and a second current on the second electrically conductive line to a first voltage and a second voltage, respectively; and
a voltage comparator for comparing the first voltage to the second voltage to provide the output.

4.   The magnetic random access memory as claimed in claim 1 wherein the resistive element is a transistor, which allows the total resistance to be set between the minimum magnetic resistance and the maximum magnetic resistance.

5.   The magnetic random access memory as claimed in claim 1 wherein the resistive element is set so as for the total resistance to be a mid-point resistance between the minimum magnetic resistance and the maximum magnetic resistance.

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6.   The magnetic random access memory as claimed in claim 1 further including a first switch coupled in series to the first electrically conductive line for enabling the magnetic memory cell to be active, and a second switch coupled in series to the second electrically conductive line for enabling the reference magnetic memory
5   cell to be active.

7.   A magnetic random access memory device comprising:
a memory array including:
        a plurality of bit lines, each bit line being electrically conductive;
10   a plurality of digit lines, each digit line being electrically conductive and perpendicularly placed to the bit lines; and
        a plurality of magnetic memory cells, one each magnetic memory cell being placed on each intersection of the plurality of bit lines and the plurality of digit lines, and being electrically coupled in series to the bit line; and
15   a reference memory array including:
        a reference line being electrically conductive;
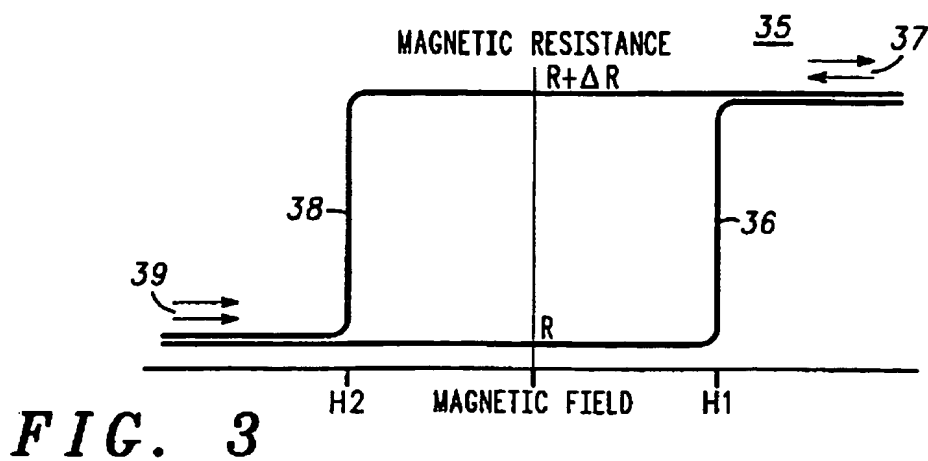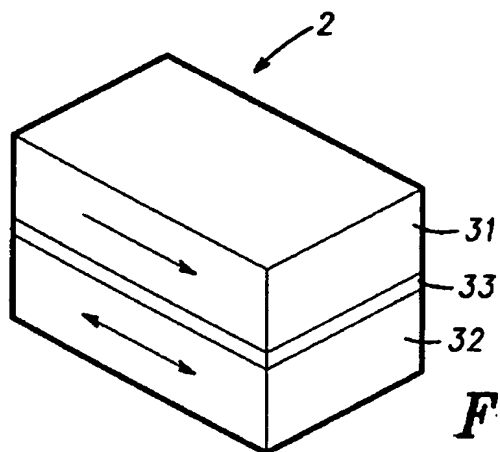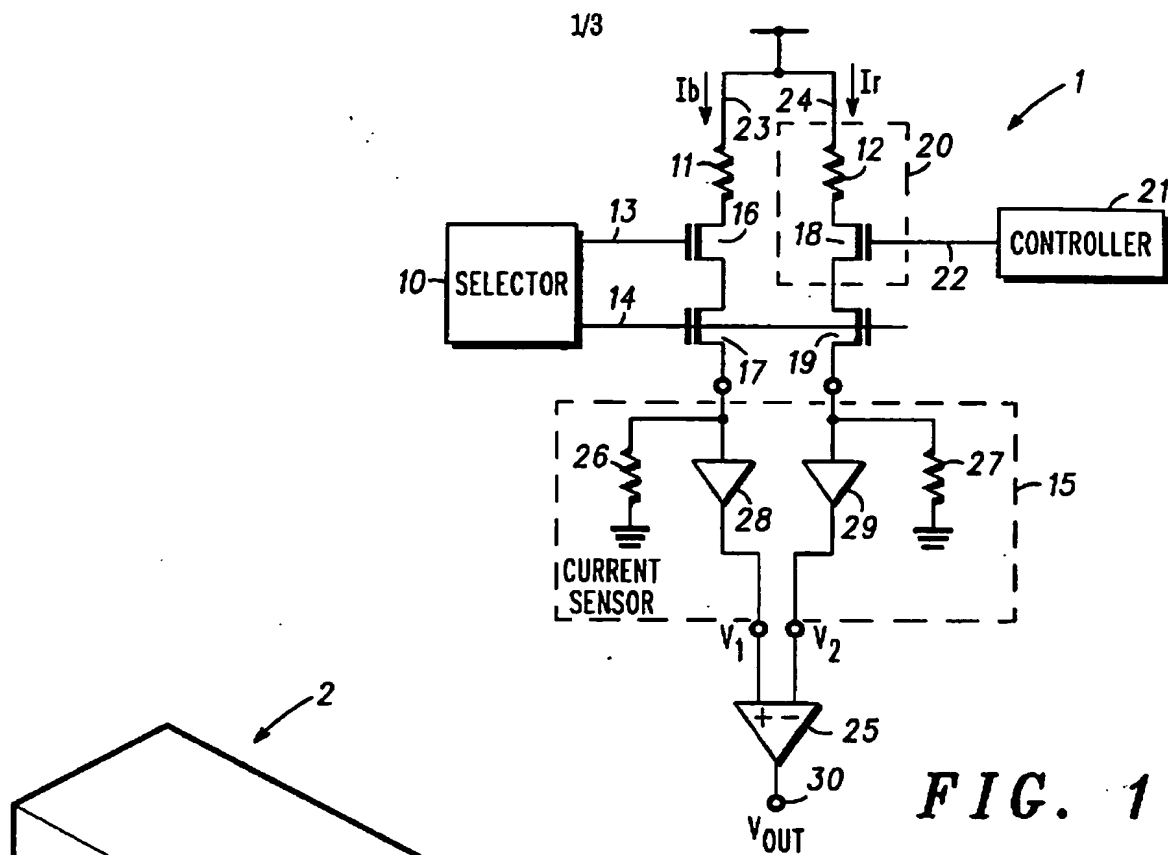   a plurality of reference bit lines, each reference bit line being electrically conductive;
        a plurality of reference magnetic memory cells, each reference magnetic
20   memory cell being electrically coupled in series to the each reference bit line; and
        a plurality of resistive elements, each resistive element being electrically coupled in series to a reference magnetic memory cell and being electrically coupled to the reference line.

25   8.   The magnetic random access memory device as claimed in claim 7 wherein each of the plurality of magnetic memory cells has a minimum resistive value and a maximum resistive value, and a total resistive value across the reference magnetic memory cell and a resistive element is set between the minimum resistive value and the maximum resistive value.
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9.   The magnetic random access memory device as claimed in claim 8 wherein the resistive element is a transistor having a gate electrode, the total resistive value being set by a reference signal applied to the gate electrode.

35   10.   The magnetic random access memory device as claimed in claim 7 wherein the magnetic memory cell and the reference magnetic memory cell have magnetic layers separated by a non-magnetic layer.
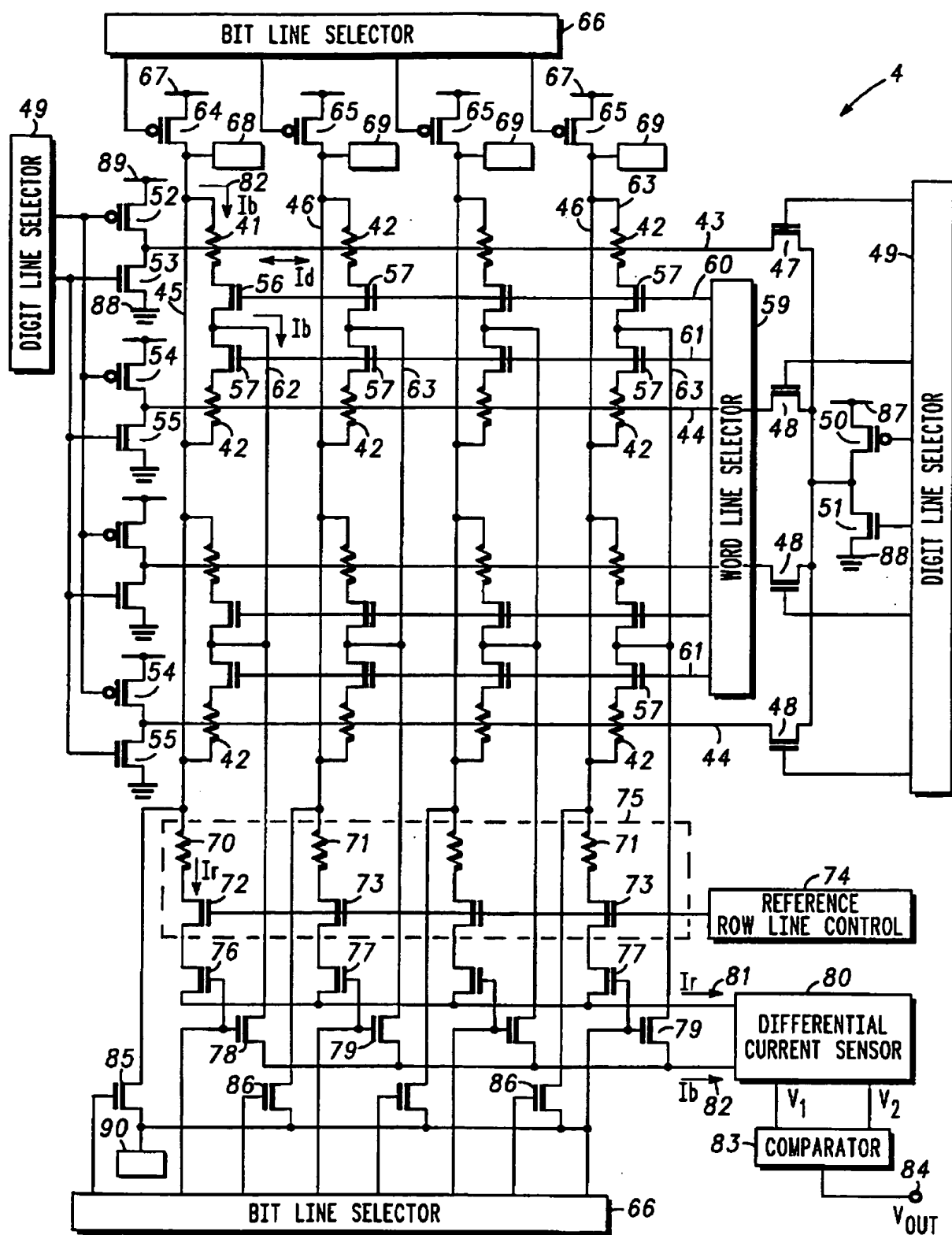
1/3

FIG. 1

FIG. 2

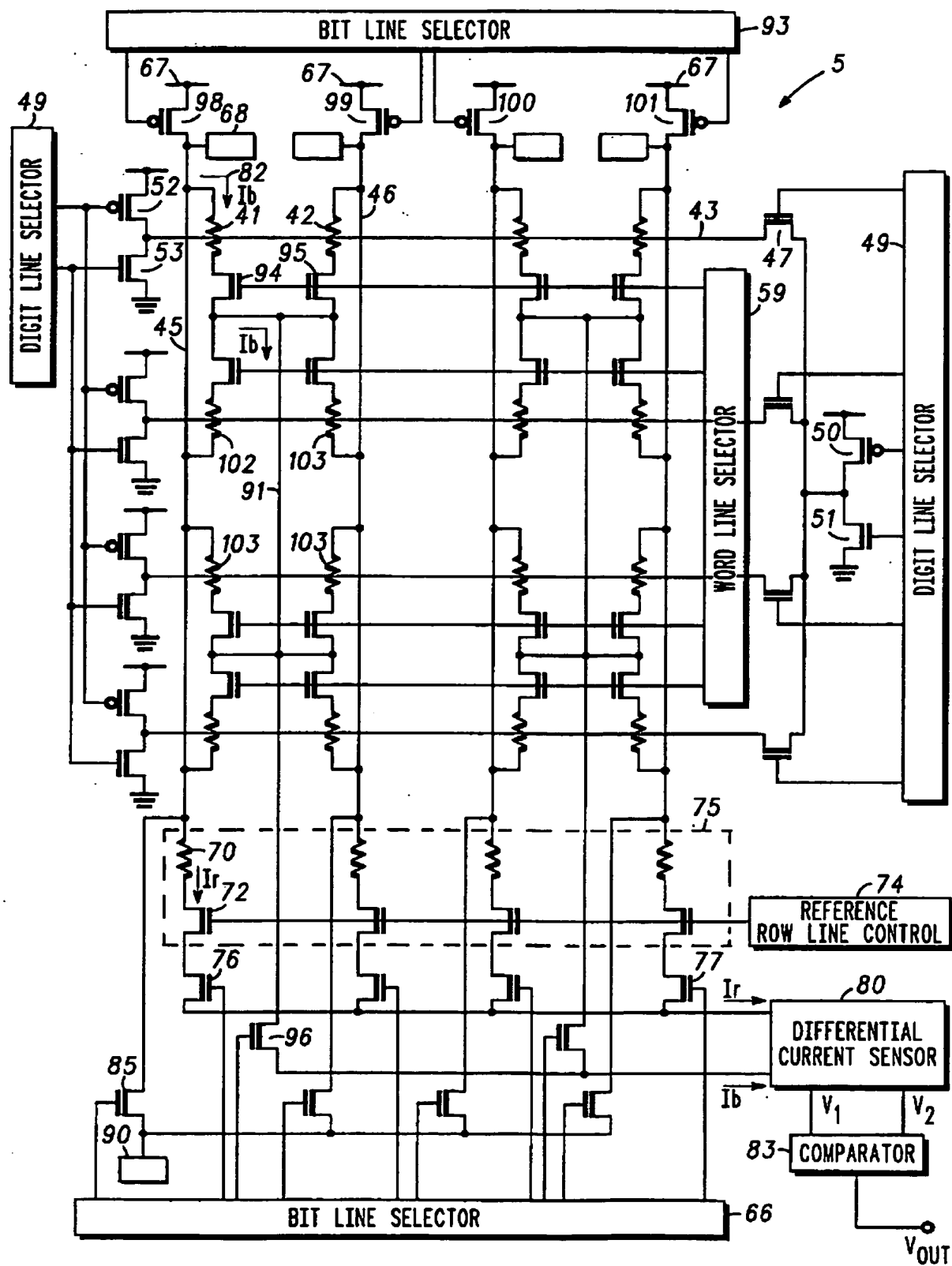
FIG. 3

FIG. 4

FIG. 5

BIT LINE SELECTOR — 93

DIGIT LINE SELECTOR — 49

WORD LINE SELECTOR — 59

DIGIT LINE SELECTOR — 49

REFERENCE ROW LINE CONTROL — 74

DIFFERENTIAL CURRENT SENSOR — 80

COMPARATOR — 83

BIT LINE SELECTOR — 66

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INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7   G11C11/16   G11C11/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 . G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 613 148 A (IBM) 31 August 1994 (1994-08-31) page 3, column 4, line 42 -page 4, column 5, line 22; figure 3 ---	1,7
A	US 5 173 873 A (WU JIIN-CHUAN ET AL) 22 December 1992 (1992-12-22) column 5, line 23 -column 6, line 45 -----	1,7

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Int. Jonal Application No

PCT/US 99/29310

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